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REMARKS

Claims 1-10 are pending in the present application. Claims 9 and 10 are currently allowed. No new matter has been added. Reconsideration is requested.

Applicants acknowledge the finding of allowability for independent claims 9 and 10.

Applicants' attorney wishes to extend his thanks for the courtesy and the consideration the Examiner extended in the interview conducted on June 20th . The following remarks provide in more detail, and with more explanation, Applicants' response to the rejections in the Examiner's Action.

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Winebarger. This rejection is hereby respectfully traversed. Applicants respectfully submit that claim 1 is not shown, taught or suggested by Winebarger and is allowable over the references of record.

Claim 1 recites:

> An under voltage detection (UVD) circuit for monitoring a supply voltage, the circuit comprising:
>
> a comparator for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage, and
>
> an integrator for time-integrating the shortfall signal to form an integrated signal,
>
> wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor.

The Examiner asserts that Winebarger discloses a comparator (identified as element 46 in Figure 2 of the reference) generating a short fall signal, and an integrator for time-integrating this shortfall signal to form a signal (indicated as elements R4 ad C2 in the reference) and that the

integrated signal is used to generate a signal for resetting a microprocessor. Further, the Examiner responds on page 10-11 of the Action to Applicants' earlier argument that the arrangement of Winebarger is not an integrator as required by Claim 1, by directing the Applicants to the disclosure of Paschal, another patent document, for further support of the premise that the Winebarger disclosure does in fact provide the required integrator operating as recited in Claim 1.

Applicants respectfully disagree with the conclusions the Examiner as presented in the Office Action. Applicants have examined Winebarger in detail and find that the reference does not show, teach or suggest the integrator as recited in Claim 1.

Considering the operation of Winebarger, in an undervoltage situation comparator 46 outputs a logical zero by actively output 58 on pulling line 61 to ground. The examiner states that the comparator outputs a shortfall signal in the terms of Claim 1, so, apparently the logical zero output by the comparator could be considered the recited "shortfall signal." This "shortfall signal" is a zero output, and so the comparator is producing no voltage, and providing no current, for the "integrator," (which the Examiner asserts is the combination of capacitor C2 and resistor R4), to be time integrated. That is, Applicants believe that in the case of an undervoltage in the arrangement of the reference Winebarger, there is simply no comparator output signal to time integrate. In fact, in this case, as line 61 is originally high, the comparator pull down (open collector) device will pull current from the capacitor C2 and from resistor R4, and so, in contrast to the time integration recited in Claim 1, the Winebarger circuit is instead discharging current and that includes current from R4 and the supply voltage, which is not "integrating".

Clearly the open collector comparator 46 of Winebarger is able only to pull its output low; the comparator cannot drive its output high. Instead the open collector circuit has to rely on

a pull up resistor (R4) for this. For further explanation Applicants enclose pages from an Electronic Engineering textbook (see the Appendix, "Electronic Principles") that depicts this kind of circuit. Thus, in the situation of the reference, the line 61 voltage (when at a low value) can only be brought to a high value via the operation of the supply voltage V+ and the R4-C2 combination, and not by any operation of comparator 46.

The RC combination of elements 68 and 70 in Winebarger has a function, it delays the voltage rise on output line 61 when the comparator is inactive by providing a time constant that controls the charging of the line by supply voltage V+ in recovering from an undervoltage. This delay is used to maintain the POR output (the logical inverse of the comparator output 58) at a high level. The charging current will flow into capacitor C2 (element 70 in Figure 2) through the resistor R4 (element 68 in Figure 2).

However, in contrast to Applicants' claimed invention as recited in Claim 1, the charging current into capacitor C2 is not due to an undervoltage (it is not the "shortfall" signal) and it is clearly not the output of the comparator 46, thus, the "integrator" identified by the Examiner is not "time integrating the shortfall signal" as specifically required by the elements of Claim 1.

Applicants conclude that the Winebarger reference does not show, teach or suggest the required elements of the independent claim, as recited above. Accordingly, Applicants believe the rejection is overcome and that Claim 1 is neither anticipated by, nor obvious over, the relied upon reference. Reconsideration and allowance over the rejection is therefore respectfully requested.

Applicants also respond to the explanation by the Examiner that the Paschal reference which is not cited as a reference but "to aid in understanding," supports his conclusion that the primary reference discloses an integrator as recited in Claim 1. Paschal, U.S. Patent No.

4,093,878, in fact supports a different conclusion about the integrator. Further, in order to provide understanding of what one skilled in the art would comprehend an "integrator" to be, Applicants are also providing an additional reference, see the "Integrator" in the Appendix.

Applicants agree that the Paschal reference does indeed illustrate an integrator circuit. However, with respect to the cited passage the Examiner quotes from, Applicants believe the Examiner may have failed to fully understand the significance of the passage. Paschal discloses in the cited portion, Col. 2 lines 38-42, "At the output of the open collector NAND gate there is provided an integrator circuit comprised of a potential source, a resistor and a capacitor, which capacitor is connected to a reference potential such as ground." The Examiner correctly states that the circuit of Paschal, and that of the primary reference Winebarger, are the same.

However, the Examiner is misinterpreting the meaning of the cited portion from Paschal. The integrator of Paschal is comprised of "a potential source, a resistor and a capacitor..". Like the open collector circuit of Winebarger, the circuit described by Paschal integrates the voltage supplied from a potential source. However, the reference does not make any statement that makes the circuit of Winebarger an integrator of the "shortfall signal" as recited in Claim 1 of Applicants' pending application. The integrator of Paschal also does not integrate the output of the NAND gate, but takes the potential from the voltage source.

Further, the Examiner cites the Paschal patent not as a reference but as a disclosure of what one skilled in the art would understand the word "integrator" to mean. However the patent was drafted by a patent attorney for the purpose of gaining a patent, and is not a document drafted by a practitioner, nor is it a reference book one skilled in the art would be aware of or look to. This disclosure seems to Applicants to be irrelevant to the point and taken out of context. The remaining disclosure of Paschal, almost entirely, is devoted to a discussion of an RC time

delay function. In this respect the Examiner is directed to Figures 1 to 6 and to the disclosure of Col. 3 line 33 to Col. 5 line 11. Figure 6 of Paschal and the corresponding text is particularly relevant. The bulk of the Paschal patent makes plain that the function of the RC combination described is to provide an RC time delay circuit. There is no other mention in the Paschal description that the output of the NAND gate of Paschal is integrated, and thus Applicants believe that the fact this was mentioned at all in the cited portion may simply be a patent attorney error.

The correct description of the RC circuit of Paschal seems to be plainly stated at Col. 3, lines 50-54:

> " An integrator circuit comprised of a series connected resistance R and a capacitor C is connected at one end to a potential source +V and at the other end to a common reference point. The juncture of the resistor R and the capacitor C is connected to the output of the NAND gate 12."

Thus, the integrator requires a series connected resistance R and a capacitor C. The disclosed NAND gate is not connected to the integrator and the integrator is not integrating the output of the NAND gate, it is integrating something else. The R and C elements of Paschal are not series-connected with respect to the NAND gate output, indeed they appear roughly connected in parallel with respect to that output.

Applicants are providing, see the Appendix, a reference also easily located on the web at http://floti.bell.ac.uk/principles/ac_intro/12%20RL%20Time,%20Integ%20&%20Diff%20-%handouts.index.htm that defines what one skilled in the art refers to as an integrator. This page is provided to aid the Examiner in understanding that the language quoted above from Paschal in

fact describes an integrator correctly, and that the NAND gate is not coupled to an integrator V; and neither is the open collector comparator of Winebarger.

Accordingly, reconsideration and allowance is again requested for Claim 1.

Claims 4-6 were rejected under 35 U.S.C. §103 as being unpatentably obvious over Winebarger. This rejection is also hereby respectfully traversed.

Claims 4, 5 and 6 each depend from and incorporate the features of Claim 1 discussed above. As argued above, Applicants believe that the parent claim is unanticipated and unobvious over Winebarger. Accordingly, each of these dependent claims recites patentably allowable elements over Winebarger and are each therefore also allowable. Reconsideration and allowance are therefore respectfully requested for these dependent claims.

Applicants also note that the Examiner admits that the relied upon reference to Winebarger does not provide the additional elements of a microprocessor; the Examiner then asserts it would have been obvious to one skilled in the art to use the reset signal of Winebarger with a microprocessor. The Examiner did not, however, provide a reference disclosing the microprocessor, instead the Examiner states it would have been *prima facie* obvious to combine the Winebarger reference with a microprocessor and to expect success. Applicants respectfully request that since no reference was provided for the remaining elements, the Examiner take official notice that it would have been obvious to provide such a microprocessor and to make the relied upon combination. The failure to provide a reference disclosing the microprocessor makes the §103 rejection untenable, as there must be a suggestion to make the combination relied upon, the Examiner has not provided the reference, so how can the Applicants determine that one skilled in the art would have been motivated to combine Winebarger with such a reference? The motivation to combine the references is a required element of the rejection and in any event

Applicants believe that the claims are not obviated by Winebarger, as the combination of Winebarger with any microprocessor still does not show, teach or suggest the elements of Claims 4-6 incorporated from Claim 1. Reconsideration is therefore requested.

Claims 1-2 and 4-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshimura in view of Woods. Applicants hereby respectfully traverse this rejection.

Applicants respectfully submit that Claim 1, the parent claim, is patentable over the combination proposed by the Examiner, Yoshimura in view of Woods.

Firstly, the proposed combination, even if made, does not show, teach or suggest the recited elements of Claim 1. As put forth by the Examiner in the Office Action, the Yoshimura reference disclosed a comparator 4 which outputs a shortfall signal upon detection of loss of power, this signal is next inverted by a buffer inverter 6 which is then fed into digital delay circuit 7. Thus, and without prejudice to Applicants' other arguments, the reference teaches that the delay circuit must be a digital delay circuit. Even if this were combined with the analogue delay circuit of Woods, as the Examiner proposed, the combination would not integrate the shortfall signal as required by Claim 1. First the delay circuit must be a digital delay as taught by Yoshimura, the RC delay of Woods does not provide a digital dealy circuit, the output of Yohsimaura's comparator is a 1, or a 0, and at Figure 1 and the corresponding text at Col. 2 line 51 and following, the reference describes in detail how the comparator and the digital delay circuit work together. Respectfully, the Applicants believe that the circuit would not work properly with a simple RC analog delay circuit substituted in Yoshimura. The waveforms of Yoshimura are illustrated in Figure 5 and are clearly digital waveforms, output C of the digital delay circuit (element 7 in Figure 1) is a digital waveform time shifted by a factor td. Applicants

conclude that because the combination does not show, teach or suggest the required elements of Claim 1, the claim is allowable.

A typical digital delay circuit provides a means for delaying the entire signal waveform; that is, the signal is effectively time-shifted by the digital delay circuit. (As evidence that this is a requirement of the digital delay circuit 7 in Yoshimura, refer to column 4, line 60 *et seq.* and Figure 5.) On the other hand, in a typical R-C analogue delay circuit, the effect of the circuit is that the rate at which the output voltage level rises to a peak is delayed; the circuit does not time-shift the entire waveform shape as in a digital delay circuit. Woods does discuss at, for example, col. 2, lines 40 to 50 that "delay circuit 130 that provides an output, voltage V_b, that is slightly delayed from its input transitions in voltage V_d". However, the person skilled in the art would take from this teaching that the delay being discussed is a delay in the rate of rise of the output voltage of the delay circuit and not a time-shift delay as provided in a digital delay circuit.

As such, the analogue delay circuit of Woods simply has no place in a digital logic circuit and would be unable to re-produce the effect desired by the digital delay circuit of Yoshimura. The exponential charging/discharge property of the R-C circuit of Woods would not provide the time-shift effect of the digital delay element of Yoshimura and is incapable of producing the Vb/Vc waveforms of Figures 5, 6 and 7 of Yoshimura.

Because there is not any reason to make the substitution, the relied upon combination proposed would not be made by one skilled in the art. There is no motivation for one skilled in the art to combine the digital circuit of Yoshimura with the analog RC delay circuit such as Woods to make the claimed invention. There is also not a chance of success if the combination were attempted in this fashion. The analogue circuit, if placed into the Yoshimura circuit, would not integrate the shortfall signal, as discussed above with respect to Winebarger, again there is no

potential to integrate in the undervoltage situation, the voltage on line b in this case is zero. Thus, there is not the required motivation nor the required chance of success to support the combination of references as a proper §103 rejection requires. Applicants again believe that for these reasons, Claim 1 is allowable, and reconsideration is therefore requested.

Applicants submit, therefore, that one skilled in the art would not combine Yoshimura and Woods, and thus Claim 1 is non-obvious over this combination of documents.

Thus, claim 1 is novel and non-obvious over all the prior art documents. Similarly, the rejected dependent claims 2 and 4-7, by virtue of their dependencies at least, are also non-obvious and allowable over the rejection. Reconsideration is therefore requested.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants requests that the Examiner contact Applicants' attorney at the address below. In the event that the enclosed fees are insufficient, please charge any additional fees required to keep this application pending, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

July 21, 2006
Date

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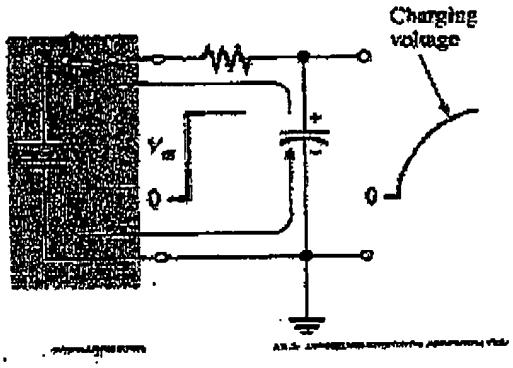
APPENDIX

Reference 1: RC Integrator
http://floti.bell.ac.uk/principles/ac_intro/12%20RL%20Time,%20Integ%20&%20Diff%20-%handouts.index.htm

Reference 2: Malvino, A.P., Electronic Principles, Sixth Edition, International Editions, 1999.

Reference 1

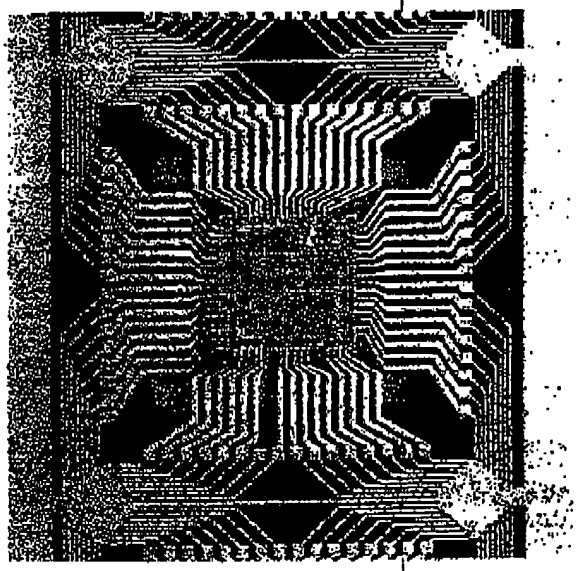
RC Integrator



- When input goes positive, capacitor will charge through resistor
- Time constant (compared to input pulse width) determines the capacitor charge

Reference 2

MALVINO
Electronic PRINCIPLES
SIXTH EDITION



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For captions describing the chapter-opening photos, see page 1011.

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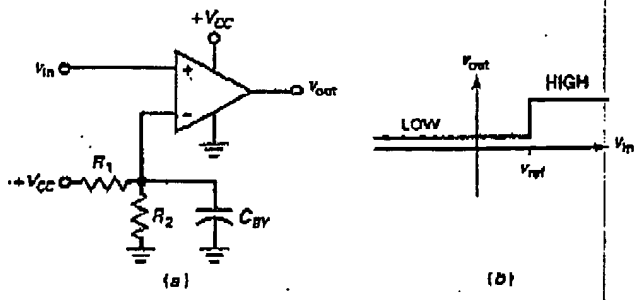


FIGURE 22-12 (a) Single-supply comparator; (b) input/output response.

op amp like an LM318. Since it has a slew rate of 70 V/μs, it can switch from $-V_{sat}$ to $+V_{sat}$ in approximately 0.3 μs.

Another solution is to eliminate the compensating capacitor found in a typical op amp. Since a comparator is always used as a nonlinear circuit, a compensating capacitor is unnecessary. A manufacturer can delete the compensating capacitor and significantly increase the slew rate. When an IC has been optimized for use as a comparator, the device is listed in a separate section of the manufacturer's data book. This is why you will find a section on op amps and another section on comparators in the typical data book.

OPEN-COLLECTOR DEVICES

Figure 22-13*a* is a simplified schematic diagram for an *open-collector comparator*. Notice that it runs off a single positive supply. The input stage is a diff amp (Q_1 and Q_2). A current source Q_6 supplies the tail current. The diff amp drives an active-load Q_4. The output stage is a single transistor Q_5 with an open collec-

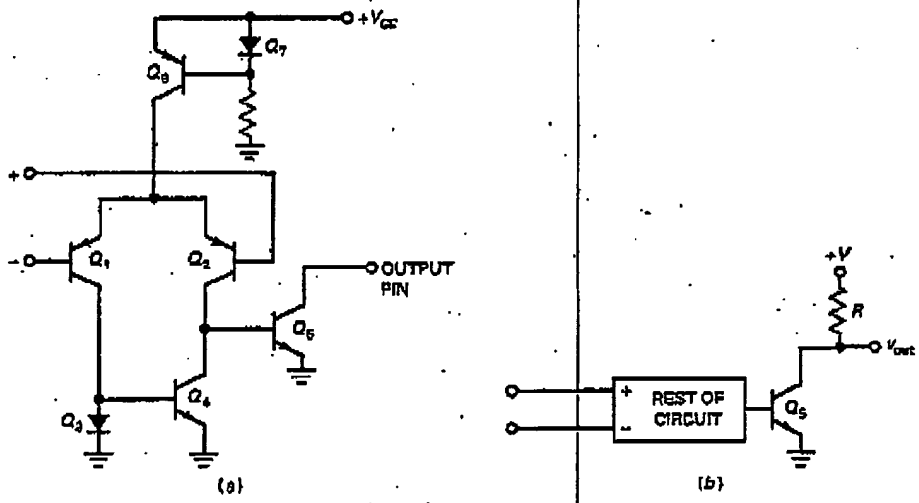


FIGURE 22-13 (a) Simplified schematic diagram of IC comparator; (b) using pullup resistor with open collector output stage.

tor. This open collector allows the user to control the output swing of the comparator.

The typical op amp discussed in Chap. 18 has an output stage that can be described as an *active-pullup stage* because it contains two devices in a class B push-pull connection. With the active pullup, the upper device turns on and pulls the output up to the high output state. On the other hand, an open-collector output stage of Fig. 22-13*a* needs external components to be connected to it.

For the output stage to work properly, the user has to connect the open collector to an external resistor and supply voltage, as shown in Fig. 22-13*b*. The resistor is called a *pullup resistor* because it pulls the output voltage up to the supply voltage when Q_5 is cut off. When Q_5 is saturated, the output voltage is low. Since the output stage is a transistor switch, the comparator produces a two-state output.

With no compensating capacitor in the circuit, the output in Fig. 22-13*a* can slew very rapidly because only small stray capacitances remain in the circuit. The main limitation on the switching speed is the amount of capacitance across Q_5. This output capacitance is the sum of the internal collector capacitance and the external stray wiring capacitance.

The output time constant is the product of the pullup resistance and the output capacitance. For this reason, the smaller the pullup resistance in Fig. 22-13*b*, the faster the output voltage can change. Typically, R is from a couple of hundred to a couple of thousand ohms.

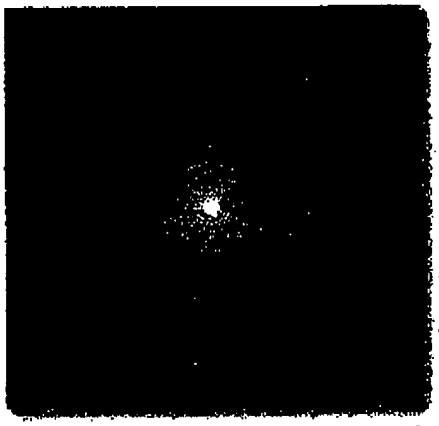
Examples of IC comparators are the LM311, LM339, and NE529. They all have an open-collector output stage, which means that you have to connect the output pin to a pullup resistor and a positive supply voltage. Because of their high slew rates, these IC comparators can switch output states in a microsecond or less.

The LM339 is a *quad comparator*—four comparators in a single IC package. It can run off a single supply or off dual supplies. Because it is inexpensive and easy to use, the LM339 is a popular comparator for general-purpose applications.

Not all IC comparators have an open-collector output stage. Some, like the LM360, LM361, and LM760, have an active-collector output stage. The active pullup produces faster switching. These high-speed IC comparators require dual supplies.

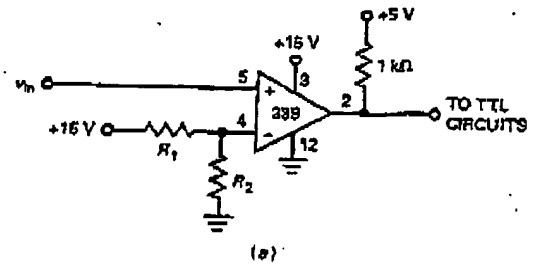
DID YOU KNOW?

You Don't Have to Have a Point to Have a Point *The basic principles of electrons were [illegible] about dispute: a particle is invisible, [illegible] negative charge, and electrons [illegible] as if concentrated in an infinitely [illegible]. But recent studies have shaken this [illegible]. Recent studies show that the apparent [illegible] of the charge of an electron may depend on a blanket of "virtual" particles around it. This cloud spreads out the electron's negative charge. Researchers who examined the collisions between electrons and positively charged positrons found that there were more collisions toward the ones with higher energy.*

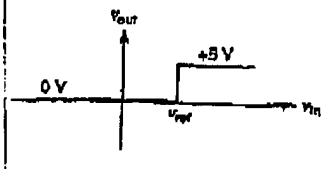


DRIVING TTL

The LM339 is an open-collector device. Figure 22-14*a* shows how an LM339 can be connected to interface with TTL devices. A positive supply of +15 V is used for the comparator, but the open collector of the LM339 is connected to a supply of +5 V through a pullup resistor of 1 kΩ. Because of this, the output swings between 0 and +5 V, as shown in Fig. 22-14*b*. This output signal is ideal for TTL devices because they are designed to work with supplies of +5 V.



(a)



(b)

FIGURE 22-14 (a) LM339 comparator; (b) input/output response.

Example 22-4

In Fig. 22-15a, the input voltage is a triangular wave with a peak value of 10 V. What is the trip point of the 339 when the input voltage is increasing? What is the trip point when the input voltage is decreasing? Use the bypass circuit. What does the output look like?